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graph TD; 110[PROVIDE COATED SILICON SUBSTRATE] --> 120[DEPOSIT ELECTRODE]; 120 --> 135[BACK-ETCH SUBSTRATE TO FORM MEMBRANE]; 135 --> 145[SPIN ON DIELECTRIC FILM]; 145 --> 155[FORM ELECTRET];
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110 PROVIDE COATED SILICON SUBSTRATE

120 DEPOSIT ELECTRODE

135 BACK-ETCH SUBSTRATE TO FORM MEMBRANE

145 SPIN ON DIELECTRIC FILM

155 FORM ELECTRET

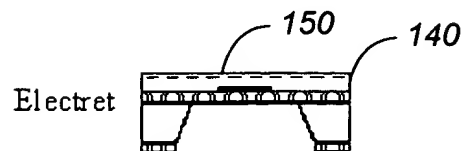
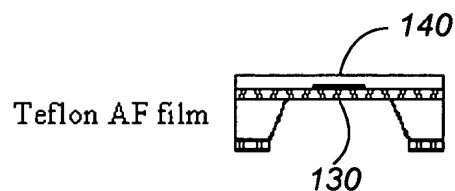
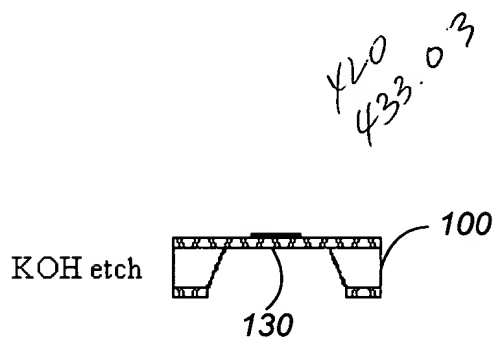
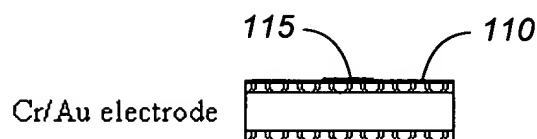
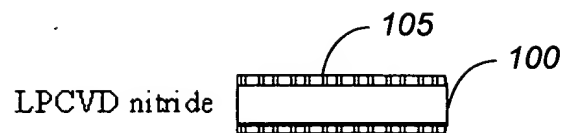
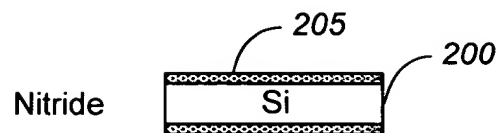
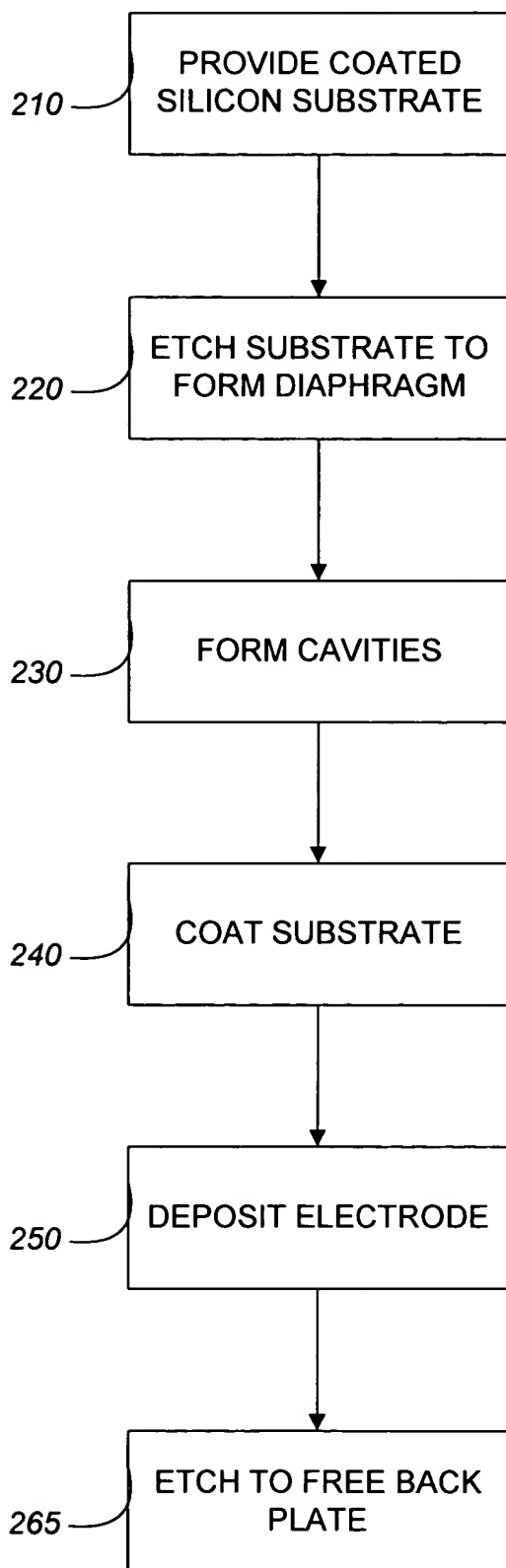
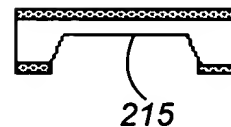


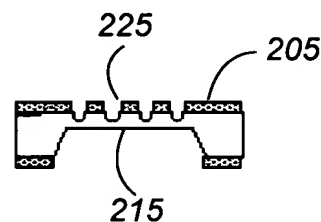
FIG. 1



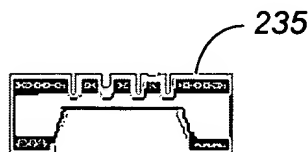
KOH etch



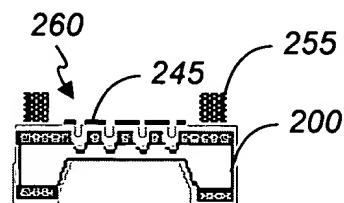
Cavity etch



Parylene Coating



PR spacer & electrode



Dicing & BrF₃ etch



FIG. 2

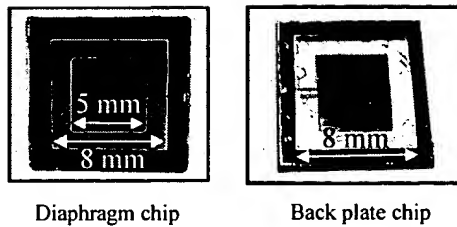


FIG. 3

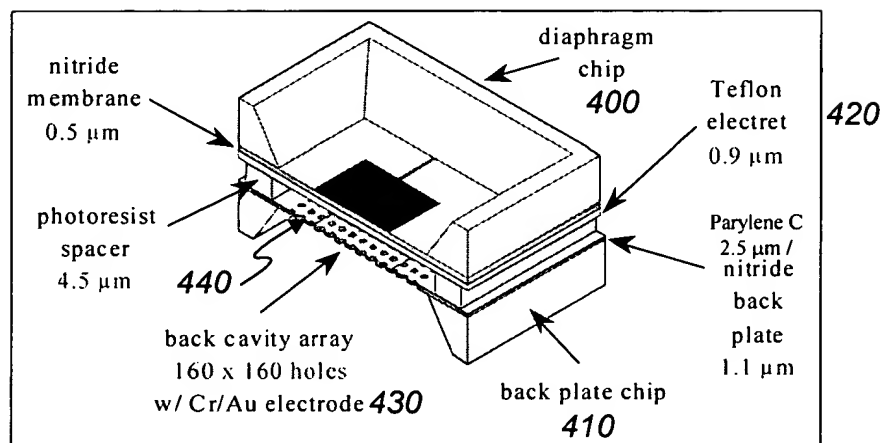


FIG. 4

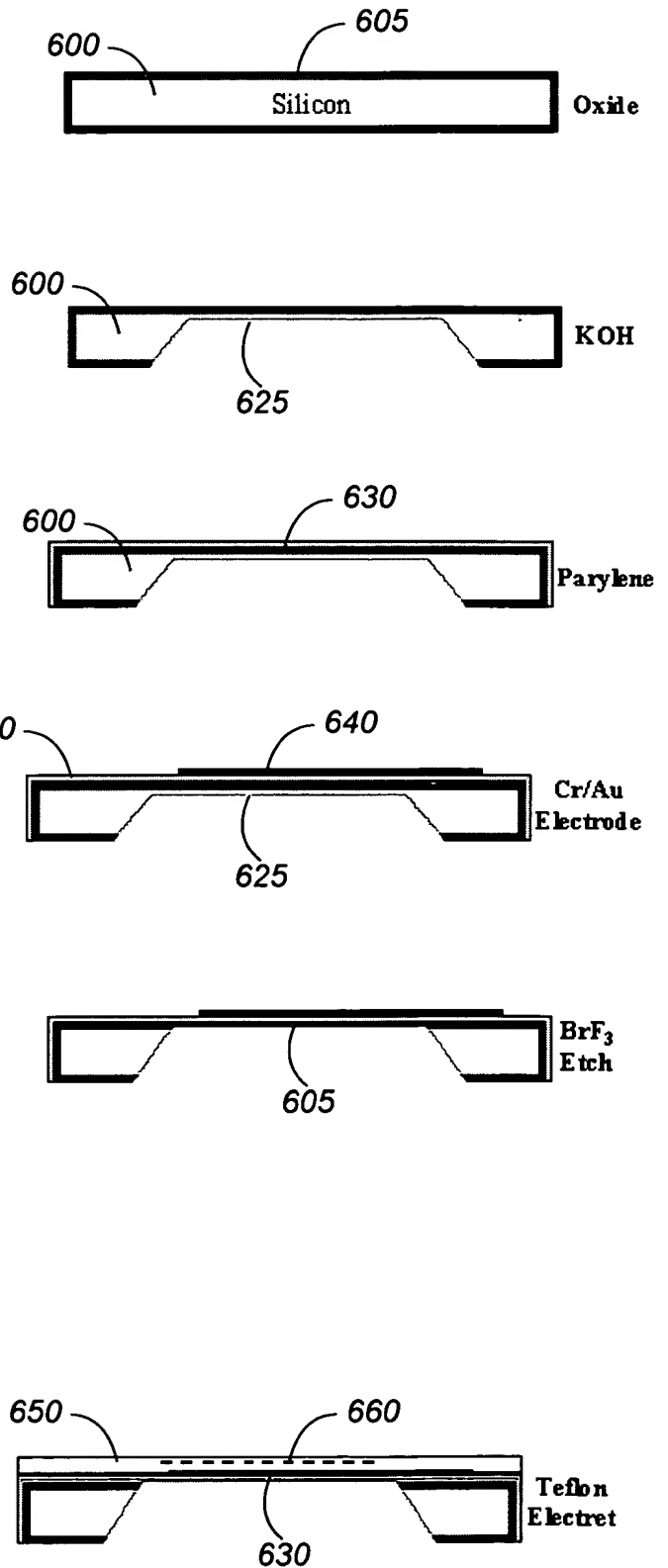
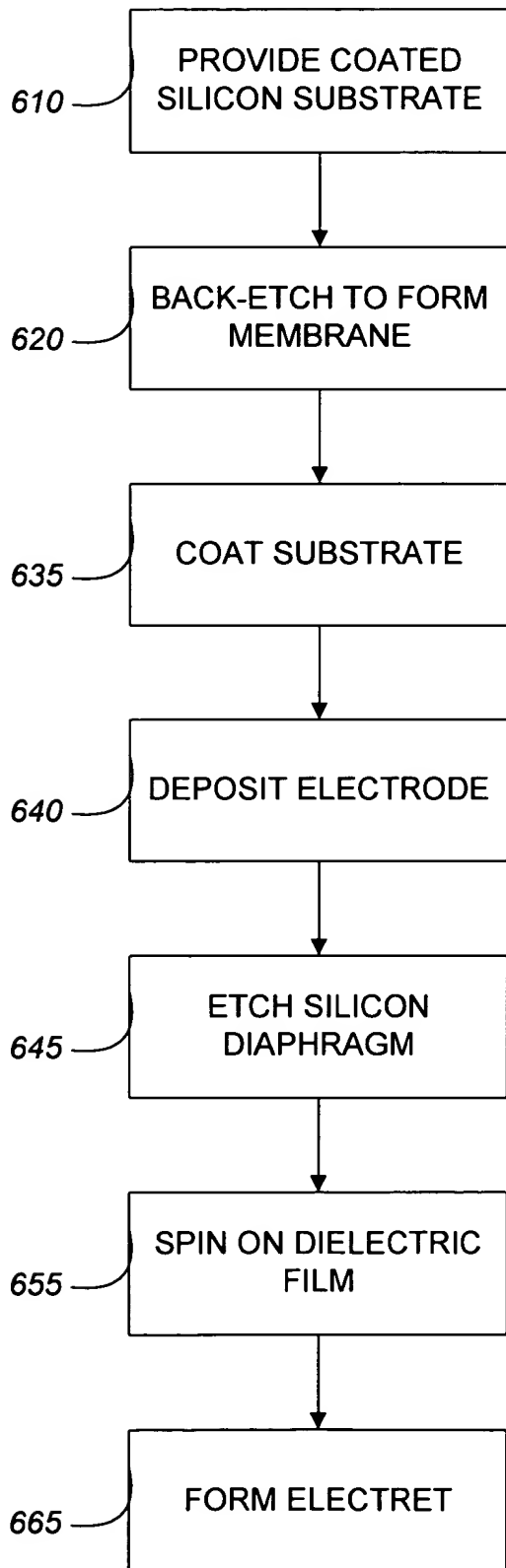


FIG. 6

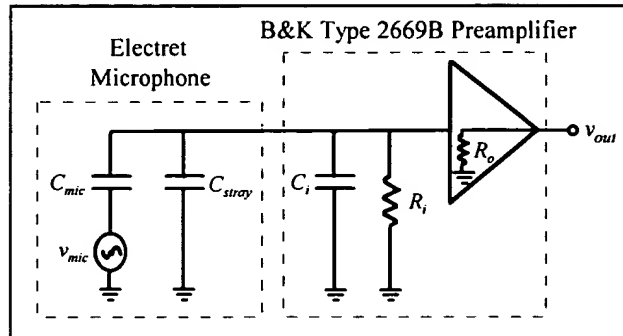


FIG. 5

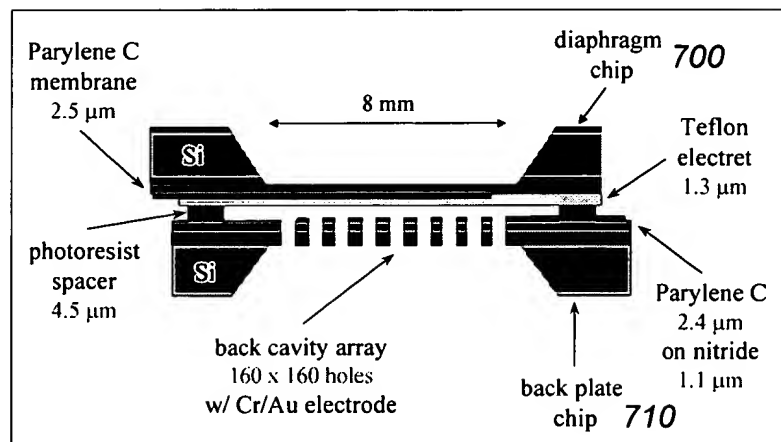


FIG. 7